20

5

WHAT IS CLAIMED IS:

- 1. A memory cell comprising:
- a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type; and a gate insulating layer formed over said substrate, the gate insulating layer
- having a first thickness formed over said first region and said second region, and a second thickness formed over said third region.
- A memory cell as in claim 1, wherein said first thickness is greater than said second thickness.
- A memory cell as in claim 1, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.
- A memory cell as in claim 1, wherein the electric field in a region of overlap between said insulating layer and said first and said second regions is between about 4 My/cm and 6 My/cm.
- A memory cell as in claim 1, wherein the electric field in a region of overlap between said insulating layer and said third region is between about 8 Mv/cm and 11 Mv/cm.
- $\label{eq:Amemory cell} 6. \qquad \text{A memory cell as in claim 1, wherein said gate insulating layer}$ $25 \qquad \text{comprises SiO}_2.$
 - A memory cell as in claim 1, further comprising a polysilicon gate electrode.
- 30 8. A memory cell as in claim 1, further comprising a control gate.
 - 9. A memory cell as in claim 1, further comprising an ONO stack.

10. A method for fabricating a memory cell, the method comprising: providing a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;

forming a first portion of a gate insulating layer over said first region and said second region; and

- forming a second portion of said gate insulating layer over said third region,
- 10 said first portion having a first thickness said second portion having a second thickness.
 - A method as in claim 10, wherein said first thickness is greater than said second thickness.
 - 12. A method as in claim 10, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.